

WAFER LEVEL PACKAGE DESIGN THAT FACILITATES TRIMMING AND TESTING

ABSTRACT OF THE DISCLOSURE

A wafer level method of packaging, trimming and testing integrated circuits is described. A wafer having trim pads is bumped before the wafer is trimmed. After the bumping, the dice on the wafer are trimmed and tested using standard trim probing and test probing techniques. After the trimming and testing, an electrically insulative undercoating is applied to the active surface of the wafer. The undercoating directly covers the trim pads while leaving at least portions of the contact bumps exposed. The undercoating may be applied using a variety of different processes, including spin-on coating, molding, screen printing or stencil printing. The undercoating may be formed from a wide variety of material including epoxy, polyimide and silicone-polyimide copolymers. With this approach, the wafer may be trimmed and final tested at substantially the same stage of wafer processing. The trimming and testing operations may be performed either sequentially or substantially simultaneously.